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Silicon-on-insulator: materials aspects and applications

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Abstract

The purpose of this contribution is to give an overview of silicon-on-insulator (SOI) technology with emphasis on the fabrication of SOI substrates and their material properties. Although the concept of SOI has been around for several decades, only recent material science advances made the fabrication of thin-film substrates possible whose material quality is comparable to bulk wafers. SIMOX wafers benefitted from lowering the oxygen dose needed for ion-beam synthesis of buried oxide layers and optimisation of the thermal annealing cycles. Through improved thinning technologies, the wafer-direct-bonding approach for the burial of thermal oxide layers became competetive for thin-film SOI, especially when complemented with the salvaging of the "sacrificial" wafer.

Keywords: Silicon-on-insulator; Wafer direct bonding; Hydrogen implantation; Layer splitting; SIMOX

1. Introduction

Most microelectronic devices utilise only a thin layer near the surface of a semiconductor wafer; in metal-oxide-semiconductor (MOS) devices, for instance, only the first few hundred nanometres from the top of the wafer are used for electron transport. The remainder of the several hundred micrometres in wafer thickness almost exclusively serves as mechanical support for the devices. Electrical interaction between devices and substrate may lead to a number of detrimental parasitic effects. In addition, the conductive bulk substrate makes the full dielectric insulation of independent neighbouring components difficult; as a consequence parasitic devices can become active. The basic idea underlying silicon-on-insulator technology is to remedy this by electrically insulating the thin layer at the wafer surface carrying the electronic devices from the bulk wafer used as mechanical support. This can be achieved either through placing the device layer onto a wafer made from an insulating material or, in a sandwich structure, through separating the device layer from the silicon bulk with an insulating interlayer (Fig. 1) [1]. Most current SOI approaches focus on the sandwich structure [1,2].

Fabricating devices in the thin device layer of an SOI substrate offers a variety of advantages, many of which result from the reduction or elimination of unwanted parasitic interactions between the devices and the bulk substrate [1]. Reduced parasitic source and drain capacitances, absence of latch-up, improved transconductance and ease of making shallow junctions are some of the main benefits. Depending on the thickness of the device layer, in thin-film SOI CMOS technology one distinguishes the fully depleted devices (the maximum depletion below the transitor gate extends throughout the device layer thickness) and par-

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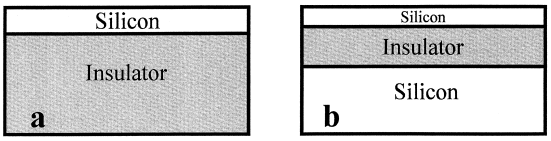

Fig. 1. The two basic SOI substrate structures: (a) Si placed on bulk insulator; (b) buried insulator layer separates the superficial Si layer from the bulk Si substrate.

tially depleted devices (film thickness is larger than the depletion. The choice of either fully or partially depleted devices affects some of the advantages SOI technology can offer.

The buried oxide layer underneath the devices reduces parasitic capacitance, especially for fully depleted devices, as seen schematically in Fig. 2 [1]. The bulk terminal capacitance consists of the capacitance between the terminal and the bulk and the capacitance between the terminal and the channel-stop implant under the field oxide. In the SOI case, however, only the capacitance between the junction and the handle wafer across the buried oxide has to be taken into account. Thus the vertical junctions made possible in SOI substantially diminish parasitic capacitances, leakage current and short-channel effects, thus increasing the speed of SOI-based devices. Additionally the inverse subthreshold slope can be steeper for fully-depleted SOI devices, allowing the use of lower threshold voltages than in bulk devices at lower leakage current. SOI-based devices consequently can operate at lower voltages without compromising the speed. Lower voltage operation reduces the overall power consumption of the devices and thus recommends SOI technology in the area of consumer electronics, especially for mobile wireless application and other hand-held devices.

The tolerance of transient radiation effects was the main driving force in early SOI development and still represents an important niche market for SOI substrates. Of the many static and transient radiation effects, single event upsets are the major radiation-induced problem in mainstream CMOS technology. As device feature sizes are becoming smaller and as the voltages are reduced, soft error rate is emerging as a major concern for server and mainframe chips; here SOI can offer an advantage. When ionising particles, for instance from cosmic rays or background radioactivity, impinge on matter they generate electron-hole pairs. In the presence of internal electric fields this results in a photocurrent which then can upset the logic state of a node. The insulating layer reduces the charge collection volume and thus increases the immunity of the devices against soft errors (Fig. 3) [1]. The reduced junction area found in SOI devices further favors the soft error immunity.

One of the drawbacks, however, of placing the devices-carrying layer onto silicon dioxide, is the poor thermal coupling to the substrate. Self-heating of the devices has become an issue in certain applications [1,3]. With only a thin device layer available, electrostatic discharge protection needs to be modified [3,4].

2. Fabrication methods

A great many fabrication methods have been investigated to date. They all aim at a thin monocrystalline silicon film on top of an insulator with defect densities as low as in bulk material. The dependence of threshold voltage on device layer thickness makes a high thickness uniformity for most electronic applications mandatory. In addition, high quality silicon/insulator interfaces are required and the insulator must exhibit good electrical characteristics.

In a certain sense, hydrogenated amorphous silicon which is usually deposited as a thin film on glass, may be regarded as a very crude approximation of a silicon-on-insulator structure. Re-crystallization of polysilicon layers deposited onto a thermal silicon oxide with laser or electron irradiation or through zone melting has been tried, also hetero- or homoepitaxy. A description of the various techniques can be found, for instance in [1]. Of the many contenders, separation-by-implantation-of-oxygen (SIMOX) and wafer direct bonding techniques currently are the front-runners, while silicon-on-sapphire, a variant of the hetero-epi-

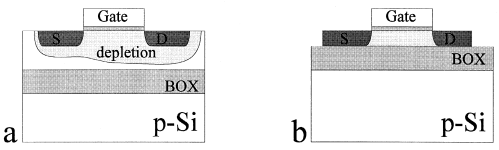

Fig. 2. (a) Partially-depleted; (b) fully-depleted mode of SOI MOSFET.

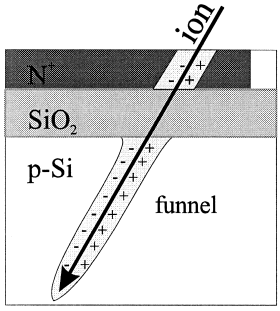

Fig. 3. BOX reduced the current associated with the energetic particle penetrating SOI device.

Table 1
Physical properties of common SOI materials

Material	Crystal structure	Lattice parameter [Å]	Rel. dielectric constant	Mean thermal expansion coefficient [K^{-1}]	Thermal conductivity [$Wcm^{-1}K^{-1}$]
Si	Diamond	5.4301	11.7	3.8×10^{-6}	1.5
$(1\bar{1}02)$ Al_2O_3	Rhombohedral	4.759	9.39	9.5×10^{-6}	0.46
SiO_2 (fused silica)	Amorphous	–	3.9	0.56×10^{-6}	0.014

taxial techniques, has established itself in the niche of radiation-hard devices.

The best compatibility with standard silicon processing techniques can be attained with sandwich structures. Silicon dioxide is the natural choice for the buried insulator although other materials like silicon nitride or oxynitride, diamond or aluminium nitride [5] have been considered. The main problem is how to bury the silicon dioxide (or other insulator chosen) under the constraints of maintaining a bulk-like quality in the device layer and high-quality interfaces between silicon and silicon oxide. The insulator currently is buried either through implantation or through wafer bonding; the relevant methods will be described in the following sections.

2.1. Silicon-on-sapphire

Silicon-on-sapphire (SOS) technology represents a subset of SOI technology of its own. Because of their composition and transparency, sapphire substrates are not compatible with standard silicon processing. Reviews on SOS technology can be found in [1,6,7] and references therein. Al_2O_3 single crystals (sapphire) are rhombohedral; for (100) silicon hetero-epitaxy, the $(1\bar{1}02)$ orientation has proved most useful [6]. The silicon layer is grown through pyrolysis of silane (SiH_4); deposition temperatures around 900–1000°C are chosen to minimise defects in silicon and simultaneously reduce the risk of autodoping with aluminium. The mismatch in lattice constant and thermal expansion behaviour (Table 1) causes a high density of crystallographic defects, especially in thin films, and compressive stress. Because of both effects the electronic properties of the device layer differ from bulk silicon. In solid-phase epitaxy and regrowth the defect density and the compressive stress are reduced through partial amorphisation of the deposited silicon layer and subsequent recrystallisation. The attractiveness of SOS for microwave circuit applications rests with the dielectric properties of sapphire (relative dielectric constant 9.39, dielectric loss tangent smaller than 10^{-4} at 3 GHz, and resistivity of 10^{-14} Ω·cm) [8]. Another advantage is the comparatively high thermal conductivity which minimises self-heating effects.

2.2. SIMOX

The prime example for the ion implantation synthesis of the buried insulator layer is SIMOX: separation by implanted oxygen [1,2,9]. SIMNI and SIMON are variants using nitrogen or oxygen and nitrogen to form silicon nitride or oxynitride as insulator. In the SIMOX process a large dose of oxygen ions is implanted into a silicon wafer which during the

post-implantation annealing react with the host to form the buried silicon oxide (BOX) layer, as schematically shown in Fig. 4. The implantation guaranties a very good thickness uniformity for both device and BOX layer across the wafer, with the device layer thickness determined by the implantation energy.

Compared to the maximum doses used in doping implantations, a 100–1000 times larger dose of oxygen is necessary to supply all the oxygen required for the buried oxide layer. Those high doses must not irretrievably damage the crystallinity of the superficial silicon layer as otherwise the subsequent annealing step could not restore the crystal quality. The amorphisation is prevented through self-annealing of the implant damage. To this end, the target substrate is kept at 500–650°C. Although those temperatures can be achieved through self-heating caused by implantation, additional wafer heating may provide a better temperature uniformity.

Because of straggling the implantation profile has a skewed Gaussian shape rather than the desired box shape. This spreading increases the critical dose which is required for obtaining a continuous stoichiometric layer at a given depth right after implantation. In the case of the common SOI structure of 200 nm device layer, 400 nm BOX thickness, for instance, a 200 keV implant with at least 1.4×10^{18} O^+/cm^2 is necessary to have a stoichiometric layer. So-called "high-dose" SIMOX material is produced with doses slightly larger than the minimum dose which would give a stoichiometric SiO_2 layer after implantation. As with increasing dose not only cost but also damage increases, "low-dose" syntheses are of current interest. There a subcritical dose creates an oxygen deficient buried silicon oxide layer. Subsequent annealing not only has to anneal defects but also to gather the spread oxygen to achieve a stoichiometric continuous silicon dioxide layer. Standard SIMOX SOI is fabricated with a high-dose process.

After the oxygen implantation the SOI structure contains a multitude of point and extended defects. The future device layer is monocrystalline; however, near the top surface there are dislocation half loops. In addition there are silicon oxide precipitates whose size increases the closer one comes to the buried oxide layer. At the top Si/buried oxide interface there are multiply-faulted defects; at the buried oxide/bulk silicon interface a heavily damaged silicon layer mainly with {113} staking faults extends somewhat into the bulk of the support wafer.

The subsequent annealing step has to transform the defective post-implantation structure into a viable substrate. Due to Oswald ripening, annealing at temperatures close to the melting point of silicon (1300–1350°C) denudes the device layer from oxygen and oxide precipitates and forms an atomically sharp top Si/SiO_2 interface. In this way, the oxygen concentration in the device layer can be as low as in float-zone grown silicon wafers. Near the bottom interface, approximately 30–200 nm long and about 30 nm thick silicon remnants are found in the oxide layer. Argon with 0.5–2% oxygen added is preferred for the annealing: the oxynitride which in a nitrogen atmosphere can form around the silicon dioxide precipitates can impede their dissolution; the oxygen protects the superficial silicon layer from pitting during the high temperatures. The high-temperature step cannot eliminate dislocations. If the dislocation density of ca 10^6 cm^{-2} is to be reduced, a cycle of implantations with subcritical oxygen does and subsequent annealing can be repeated until the required dose has been reached. As the dislocation generation increases with implantation dose, multiple lower-dose implants can keep the dislocation density well below 10^3 cm^{-2} and avoid the silicon islands in the BOX layer. Lower implantation doses are attractive not only from the vantage point of implantation damage but also for throughput and cost considerations. Through a judicious choice of annealing rates and temperatures, the precipitation behaviour (nucleation, growth or ripening) of the silicon oxide precipitates can be controlled in such a way as to

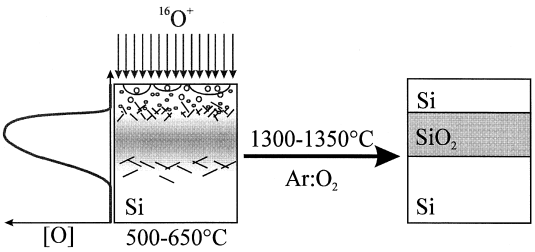

Fig. 4. Principle of SIMOX process. Dislocation half-loops, oxide precipitates, multiply faulted defects and {311} defects are schematically indicated.

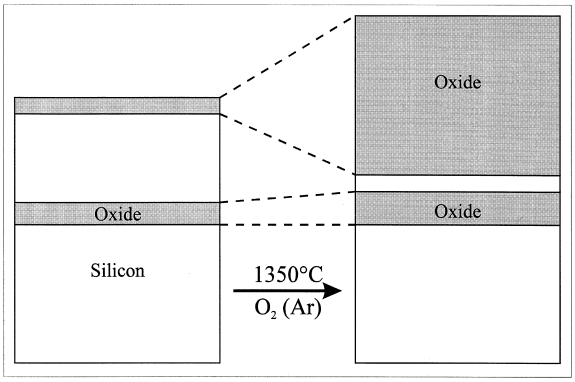

Fig. 5. Principle of the ITOX process.

obtain stoichiometric SiO_2 layers from subcritical implantation doses in the 10^{17} cm^{-2}. For a given annealing sequence, apparently only a small "window" of implantation doses guarantees a continuous silicon dioxide layer after annealing. Usually in SIMOX material, the thickness of the BOX solely depends on the implanatation dose. Nakashima et al. [10] proposed to increase the BOX thickness at the expense of the device layer thickness through dry thermal oxidation in a mixture of argon and oxygen of the superficial silicon layer at 1350°C, a process they termed ITOX (internal oxidation) (Fig. 5). Recent progress in this field has been summarised in [11].

A typical SIMOX defect is the so-called "HF defect". When the device layer is exposed to hydrofluoric acid, silicide or silicate inclusions are being etched until the BOX is exposed. Dissolution of the oxide at those spots then reveals the defective spots. HF defect densities less than 1 cm^{-2} now are standard. Pinholes (silicon pipes) in the BOX are attributed to particles on the wafer surface which mask the underlying material during implantation. Pipe densities are less than 0.2 cm^{-2}. In addition, SIMOX oxides tend to differ from thermally grown surface oxides in their excess silicon content.

2.3. Wafer direct bonding approaches

Wafer direct bonding [12] offers an alternative way to create the buried oxide layer. A thermally oxidised silicon wafer is bonded to another oxide-covered silicon wafer. This joining technique utilises the phenomenon that two solids with mirror-polished flat surfaces, when brought into intimate contact, stick to each other. In the case of the oxide-covered wafers, the wafer surfaces are silanol-terminated. The attraction between the two wafers primarily is the result of hydrogen bonding between the chemisorbed water layers. As this initial adhesion is too weak for the subsequent thinning, the bonded pair is annealed at high temperatures to achieve sufficient mechanical strength. During this fusion process the two oxide layers react with each other to form the BOX. Subsequently one wafer is thinned down to the desired thickness of the device layer. The required thickness of the device layer usually may take any value between some 50 nm up to 100 μm, depending on the specific SOI application in mind. The thickness and uniformity of the BOX is essentially controlled through the thermal oxide growth.

The SOI fabrication techniques utilising wafer bonding [1,2,12] mainly differ in their choice of thinning technique. One can distinguish between the bond-and-etch-back approaches and the layer splitting techniques. The bond-and-etch-back methods can be divided into those using no etch-stop and those which do; the latter may be subdivided according to the etch-stop chosen. The future device layer on the sacrificial layer can be transferred to an arbitrary substrate. This opens the possibility to fabricate SOI substrates with other materials than silicon, like fused silica (quartz) or silicon carbide, as handle wafers. Traditional wafer-bonding-based SOI fabrication techniques consume two silicon wafers for one SOI substrate although more recent concepts based on ion-beam sectioning techniques inspired by an idea of M. Bruel [13] allow the salvage of the "sacrificial" wafer. As a result of wafer edge rounding effects, all bonded SOI wafers have an edge exclusion of around 2 mm in common.

2.3.1. BESOI

The bond-and-etch-back (BESOI) methods in their simplest form start with one wafer carefully oxidised so as to minimise defects at the interface between silicon and silicon dioxide and another oxide-covered silicon wafer (Fig. 6) [14]. After annealing, the originally oxidised wafer is mechanically thinned to the desired thickness. Accurate thickness mapping combined with numerically controlled local plasma-assisted chemical etching (PACE) may allow the thinning of the device layer down to less than 100 nm with a thickness variation of less than 10 nm, depending on the waviness of the initial wafer. To improve the thickness uniformity of the device layer, various etch-stops have been tested [12]. The etch-stop layer separates the future device layer from the remainder of the wafer. During the thinning process, the etch-stop protects the device layer until the sacrificial wafer has been removed. The removal of the etch-stop then leaves a uniform device layer. As a compensation for the limited selectivity of the etch-stops, a double etch-stop has frequently been proposed. Nowadays the BESOI methods are mainly reserved for the fabrication of thick layer SOI substrates for which the simple grind-and-polish approach is sufficient.

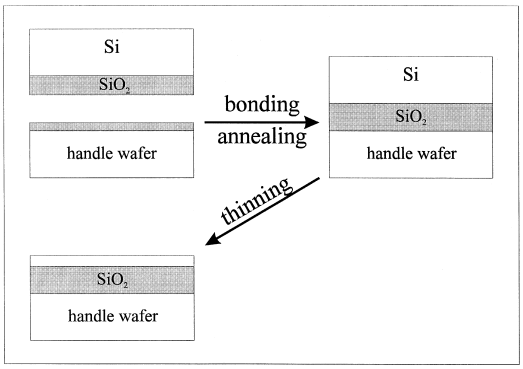

Fig. 6. Principle of the bond-and-etch-back approach.

2.3.2. ELTRAN

The epitaxial layer transfer (ELTRAN®) exploits the high etch-selectivity (ca 10^5) between porous and non-porous silicon in a $HF–H_2O_2$ etchant (Fig. 7) [15]. A sacrificial p^+ silicon wafer (up to 300 mm diameter) is anodised, without edge exclusion, in a 2:1 mixture of 49% hydrofluoric acid and ethanol to form a 10–20 μm thick layer of porous silicon. This layer is the only etch stop needed. The porous silicon is slightly oxidised at low temperatures before the surface oxide is removed with HF. A prebake in 760 Torr hydrogen prepared the porous silicon for epitaxy. In a mixture of SiH_2Cl_2 and H_2 a silicon film was grown epitaxially on top of the porous layer through chemical vapour deposition. Then a thermal oxide is grown on the epitaxial layer. After bonding the wafer to another oxidised silicon wafer, the pair were annealed at temperatures up to 1180°C. Mechanical thinning of the sacrificial wafer exposed the porous silicon layer which is etched in a hydrofluoric acid–hydrogen peroxide mixture. The etched surfaces are annealed in hydrogen at atmospheric pressure at temperatures above 1000°C, so as to smooth the surface and to reduce the boron concentration of the device layer through out-diffusion below 5×10^{15} cm^{-3} [16]. Surface roughness comparable to prime grade bulk wafers is achieved without polishing. The HF-defect density is lower than 0.05 cm^{-2}.

Here, as epitaxial silicon is being offered, grown-in defects like crystal originated particles are not an issue. With respect to crystal quality, the method therefore has the potential to outperform any SOI fabrication technology relying on bulk silicon.

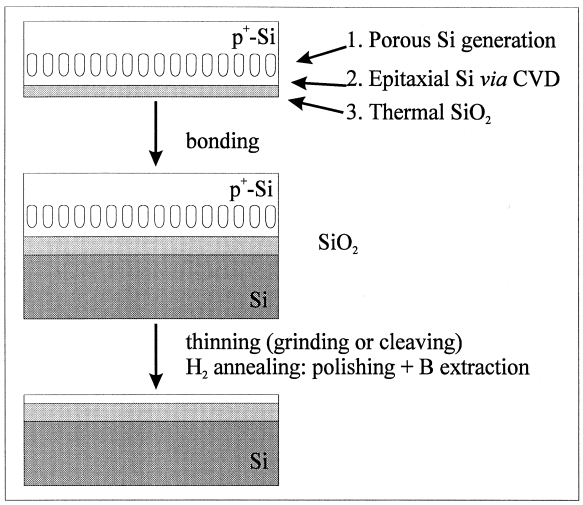

Fig. 7. ELTRAN: Epitaxial Si layer transferred onto Si through direct bonding. The porous Si layer serves as etch stop, and may be used as a cleavage plane to salvage the sacrificial wafer.

2.3.3. Ion beam cutting

The layer-splitting approaches are inspired by an elegant idea of Bruel who "married" implantation with wafer direct bonding so as to combine the thickness control afforded by ion implantation simultaneously with the performance of thermally grown oxides [13,17]. This wafer-scale ultra-microtomy is usually referred to as exfoliation or "smart cut". However, strictly speaking Smart Cut® refers to a proprietary process sequence, and alternative suggestions as to how to realise the layer splitting have been demonstrated successfully [27]. The principle behind Bruel's idea is deceptively simple (Fig. 8). As is well known from the study of nuclear reactor materials, excessive irradiation with ions can make a material blister at its free surface. By stiffening the surface through bonding a second wafer to the implanted surface, the radiation damage results in layer-splitting rather than in blistering. For the silicon-on-insulator fabrication, hydrogen is implanted through the future buried oxide layer into the silicon wafer, typically at a dose of 2×10^{16}–1×10^{17} cm^{-2} protons [13]. The choice of implantation energy defines the thickness of the device layer (about 8 nm/keV in silicon). On annealing after wafer bonding, the pressure built up during ripening and hydrogen precipitation of the implantation-induced microvoids splits the implanted silicon wafer in the damage layer. After a second annealing step and a final "touch polishing" which removes only some tens of nanometres of the device layer, the surface and crystal quality of the SOI wafer's device layer is comparable with commercial bulk wafers [18]. The necessity of smoothing the split surfaces limits the minimum thickness attainable through the standard splitting process. Besides the thickness uniformity of ca. 10 nm, the great benefit afforded by this splitting technique is its economy, as after polishing, the split wafer can be salvaged, either for use as handle wafer or for another ion-beam sectioning. Whereas traditionally bonding-based SOI fabrication methods consumed two silicon

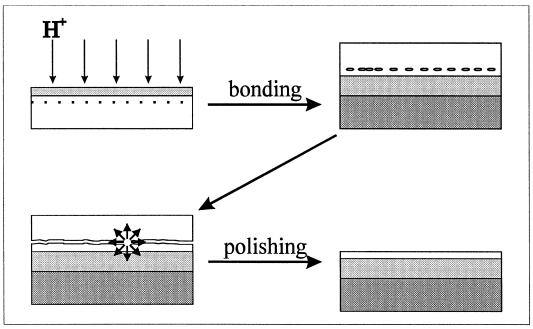

Fig. 8. Principle of ion-implantation based on the layer-splitting techniques.

wafers to give one SOI substrate, the combination of wafer bonding with ion implantation in the layer splitting approach effectively produces one SOI wafer for each silicon wafer used, a concept now transferred to ELTRAN wafers, too [19]. The SOI-wafers fabricated with a Smart Cut® technique are offered under the tradename Unibond, in all standard silicon wafer diameters up to 300 mm [18]. Sometimes "unibond" is used to refer generally to the layer splitting techniques for fabricating SOI substrates.

A variant known under the name "genesis process" uses plasma immersion ion implantation, low-temperature plasma-wafer-bonding and room temperature splitting [20]. Here, the splitting is induced mechanically: a nitrogen beam blown at the implant damage layer. The low-temperature cleavage in the plane of hydrogen-implantation-damage results in low surface microroughness [20]. The layer-splitting techniques are not restricted to the fabrication of silicon-on-insulator substrates for which they were originally developed. The realisation that an ever wider variety of materials may be split with this novel microtomy technique opens up new possibilities for material combination and a diversification of thin single crystals on insulator schemes. Silicon-on-quartz (fused silica) for instance, can be produced in this way [21]. Even other semiconductors like SiC, GaAs etc can be used as a device layer. This increases the possibilities to optimise the structures for particular applications like radio-frequency devices, radiation-hard devices, or power electronics.

Recently, SOI-substrates based on the SIMOX or on the smart cut process have been compared with respect to their electrical properties, e.g. [22–24]. In addition, the self-heating effect has been compared for SIMOX and Unibond substrates [25].

3. Applications

So far SOI substrates have mainly found application in niche markets for radiation-hard devices, for devices working at high temperatures and for power devices. The appeal for mainstream IC fabrication on thin-film SOI substrates comes from the possibility to reduce the power consumption, to increase the speed of the devices and of extending the usability of current process technology to next generation device performance. Because in fully-depleted devices their performance is severely influenced by the quality of the Si/SiO_2 interface, frequently the partially-depleted mode of operation is preferred [3,4]. In that mode, floating body effects require modifications of circuit design, as e.g. discussed in [3]. The benefits of SOI have been utilised for logic devices, static or dynamic random access memories (SRAMs or DRAMs) or flash memories. RF applications have been an important niche for SOI in the form of silicon-on-sapphire. Because of the compatibility with standard processing technology, SOI with buried oxide layers on high-resistivity silicon or silicon-on-quartz would be advantageous alternatives.

In addition to its use as electronic substrate, SOI wafers are also a commercially available convenient material for silicon surface micromachining [26]. There, selective etching is used to fabricate sensors and integrated optics. In silicon surface micromachining, structures are formed from thin layers deposited or grown on the superficial silicon layer. The BOX layer functions as sacrificial etch-stop with high selectivity against device layer and substrate. Simultaneously, the BOX layers can be used as electrical insulation or as spacer layer. The device layer provides mechanical and electrical properties of bulk-like quality which polysilicon layers grown on oxidised silicon cannot offer, and the handle wafer acts as mechanical support. Device and BOX layer thicknesses can be chosen as the design requires. An additional advantage of SOI substrates as starting material for silicon surface micromachining is the compatibility with microelectronic technology permitting the integration of the mechanical device into a microelectromechanical system (MEMS).

4. Summary

Silicon-on-insulator wafers are now available in all current silicon wafer sizes, with device layers apparently in bulk-like quality. In the case of SIMOX wafers, lowering of the implantation dose reduced the residual damage in the device layer, and a better understanding of the growth process of the silicon dioxide layer improved the quality of the BOX and of the Si/SiO_2 interface. Through improved thinning technologies, the wafer-direct-bonding approach for the burial of thermal oxide layers became competetive for thin-film SOI, especially when complemented with salvaging the "sacrificial" wafer. Since the successful implementation of the layer splitting approach, the conventional BESOI techniques have no longer been seriously considered for the fabrication of thin-film SOI substrates, used for mainstream electronic applications. BESOI has been restricted to the fabrication of SOI substrates with thick layers of silicon. The use of epitaxial silicon in the ELTRAN approach gives this technique the potential to outperform all other SOI approaches which rely essentially on bulk silicon with its inherent defects. At present, SIMOX and the smart-cut related bonded SOI wafers present the most mature SOI substrates. Recently, IBM committed itself to mass production on SOI substrates. They will use

partially-depleted devices in silicon films more than 0.15 μm thick. Although IBM initially will use SIMOX wafers, SOI substrates produced with other techniques currently are being evaluated, too. IBM embarking on SOI technology for mainstream IC fabrication amounts to a final breakthrough for SOI technology, irrespective of the technique chosen for fabricating the substrate. Much of SOI technology will depend on how IBM fares with its SOI lines.

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