## Silicon based 3D-nanomachining for wafer-scale fabrication of nano-devices

## tutorial

May 29<sup>th</sup>, 2019 | 4:00 pm Lecture Hall MPI | B.1.11

## Abstract

Effectively addressing the third dimension has become an important challenge in silicon based technology, both to increase the areal density of components as well as to realize new functionalities. In this tutorial I will introduce new strategies to fabricate functional 3D-nanostructures by combining the crystallographic properties of the silicon wafers with advanced nano-patterning techniques like edge – and corner lithography. Using these strategies it is possible to fabricate 3D structures with essential dimensions in the sub-20 nm regime, while using relative low resolution lithography to define the position and density of these structures.

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I will explain our exploration of the 3D application of these patterning techniques. An important concept that will be introduced is the so-called "self-multiplying" or "fractal" fabrication sequence, which enables the self-aligned increase of feature density. The tutorial will be concluded with examples of nano-devices that have been or can be created using the introduced concepts.

