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DESIGN, MANUFACTURING, AND MODELLING CHALLENGES FOR VERY LARGE-SCALE INTEGRATED QUANTUM PROCESSORS IN FOUNDRY CMOS TECHNOLOGIES

ABSTRACT

This presentation will discuss the main challenges in the physical implementation, design, hierarchical modelling and simulation of the scalable qubit array and of the cryogenic control and readout electronics for future Quantum Processors with millions of qubits manufactured in commercial FDSOI and FinFET foundry technologies. Impact of process manufacturing rules restrictions and process variation on qubit design and modelling, circuit heat dissipation and layout miniaturization to fit the qubit array pitch, qubit-to-qubit crosstalk, and the need for atomistic, classical, and behavioural qubit simulation and modelling will be covered in detail.

**SEPTEMBER 25,
2023,**

2:00 PM

LECTURE HALL

